In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) An integrated circuit, comprising:

an input port by which data is received from a source external to the integrated circuit;

a configurable logic array having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array;

memory ~~adapted to store~~ storing instructions for a mission function for the integrated circuit, ~~to store~~ and storing instructions for an initialization function used to transfer the configuration data to the programmable configuration points within the configurable logic array in response to an initialization event; and

a processor coupled to the memory which fetches and executes said instructions from the memory.

2. (original) The integrated circuit of claim 1, including:

a programmable configuration memory on the integrated circuit adapted to store the configuration data, wherein said initialization function transfers the configuration data from the programmable configuration memory to the configurable logic array.

3. (original) The integrated circuit of claim 1, wherein said memory comprises a non-volatile store.

4. (original) The integrated circuit of claim 1, wherein said memory comprises a floating gate memory store.

5. (original) The integrated circuit of claim 1, wherein said memory comprises a read-only memory store.

6. (original) The integrated circuit of claim 1, wherein said memory comprises a first non-volatile store for the initialization function, and a second store for the mission function.

7. (original) The integrated circuit of claim 1, wherein said memory comprises a first volatile store for the initialization function, and a second store for the mission function.

8. (original) The integrated circuit of claim 1, including a watchdog timer coupled to the processor, and wherein the initialization function includes using the watchdog timer to generate an initialization event in response to errors, and upon the initialization event, re-executing the initialization function.

9. (original) The integrated circuit of claim 1, including a watchdog timer coupled to the processor, and wherein the initialization function includes loading the configuration data onto the integrated circuit via the input port on the integrated circuit and using the watchdog timer to generate an initialization event in response to errors, and upon the initialization event, reloading the configuration data via the input port.

10. (original) The integrated circuit of claim 1, wherein the initialization function includes receiving encrypted configuration data via the input port on the integrated circuit, and decrypting the configuration data.

11. (original) The integrated circuit of claim 1, wherein the initialization function includes receiving compressed configuration data via the input port on the integrated circuit, and decompressing the configuration data.

12. (original) The integrated circuit of claim 1, wherein the electrically programmable configuration points comprise non-volatile, charge programmable memory cells.

13. (original) The integrated circuit of claim 1, wherein the electrically programmable configuration points comprise nonvolatile, programmable memory cells.

14. (original) The integrated circuit of claim 1, including:

an interface between the processor and the configurable logic array supporting said initialization function.

15. (original) The integrated circuit of claim 1, wherein said memory stores instructions for an in-circuit programming function to write or modify instructions for the initialization function.

16. (original) The integrated circuit of claim 1, wherein said memory includes a protected memory array storing instructions for a backup configuration load function, and a second memory array storing instructions for said initialization function, the protected memory array being protected from alteration by an in-circuit programming function and the second memory array being accessible to be written or modified by the in-circuit programming function.

17. (original) The integrated circuit of claim 1, wherein said processor comprises a configurable logic array configured to execute said instructions.

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